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**Kim et al.**

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(54) **ORGANIC LIGHT EMITTING DISPLAY  
PANEL AND METHOD OF  
MANUFACTURING THE SAME**

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See application file for complete search history.

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<b>H01L 33/08</b>	(2010.01)
<b>H01L 51/56</b>	(2006.01)
<b>H01L 51/00</b>	(2006.01)

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(52) **U.S. Cl.**

CPC ..... **H01L 51/5203** (2013.01); **H01L 27/3246**  
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**51/0005** (2013.01); **H01L 51/56** (2013.01);  
**H01L 2227/323** (2013.01)

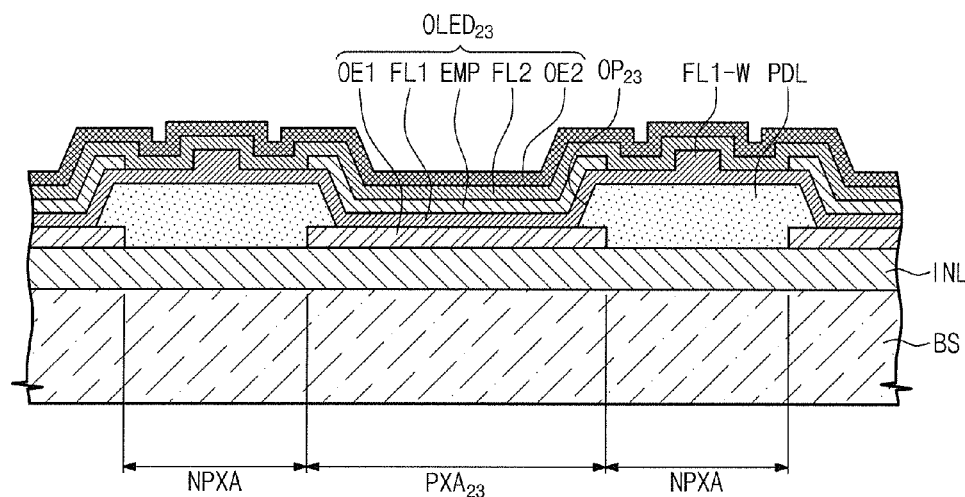
(57) **ABSTRACT**

An organic light emitting display panel including a partition  
wall to prevent different organic light emitting materials from  
being mixed with each other between adjacent light emitting  
areas. The partition wall may protrude from a surface of a  
pixel definition layer or a first common layer. Accordingly,  
desired light colors are generated by organic light emitting  
patterns respectively disposed in the light emitting areas.

(58) **Field of Classification Search**

CPC ..... H01L 27/3246; H01L 27/3283; H01L  
27/3295

**8 Claims, 18 Drawing Sheets**



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Fig. 1

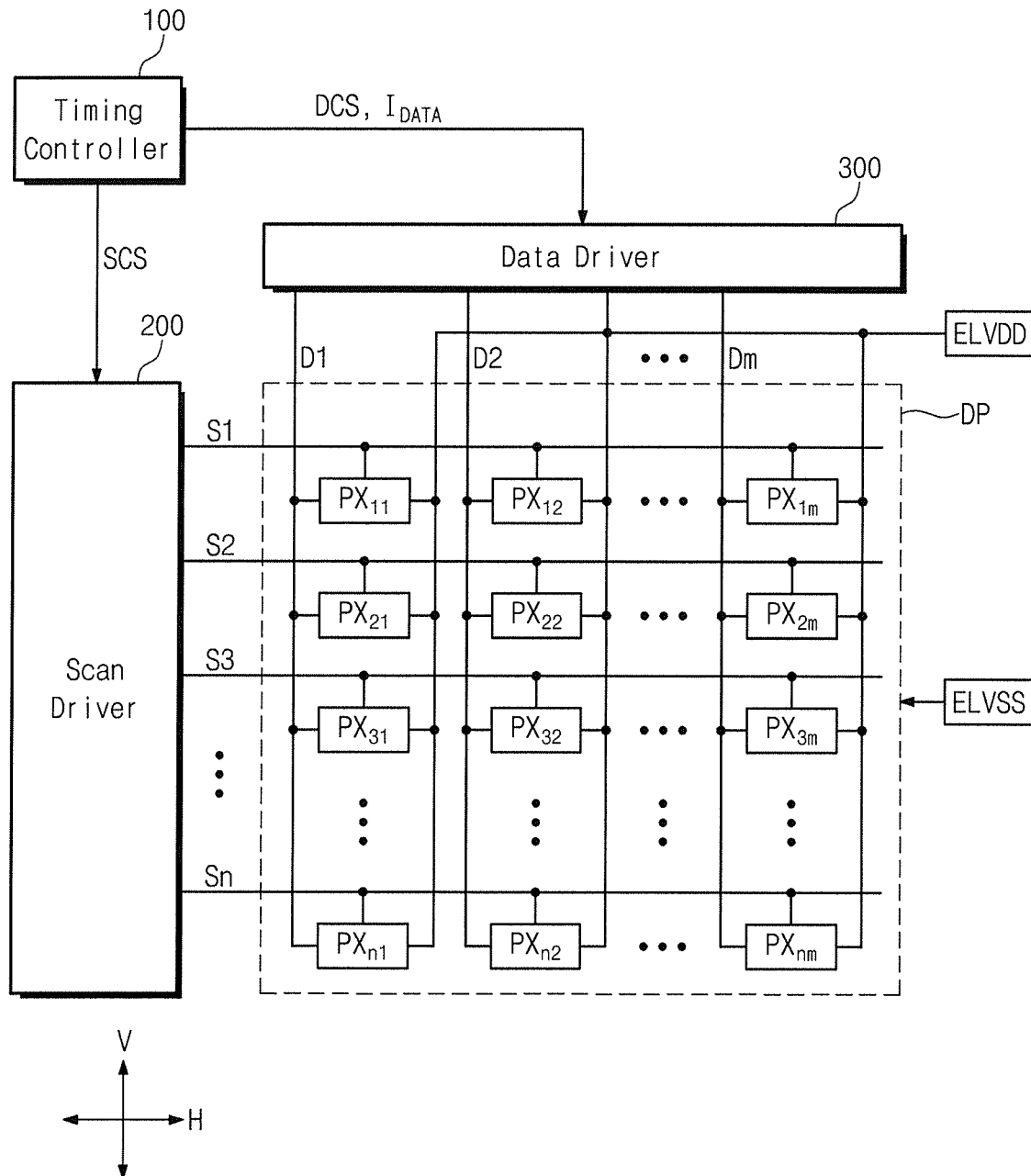


Fig. 2

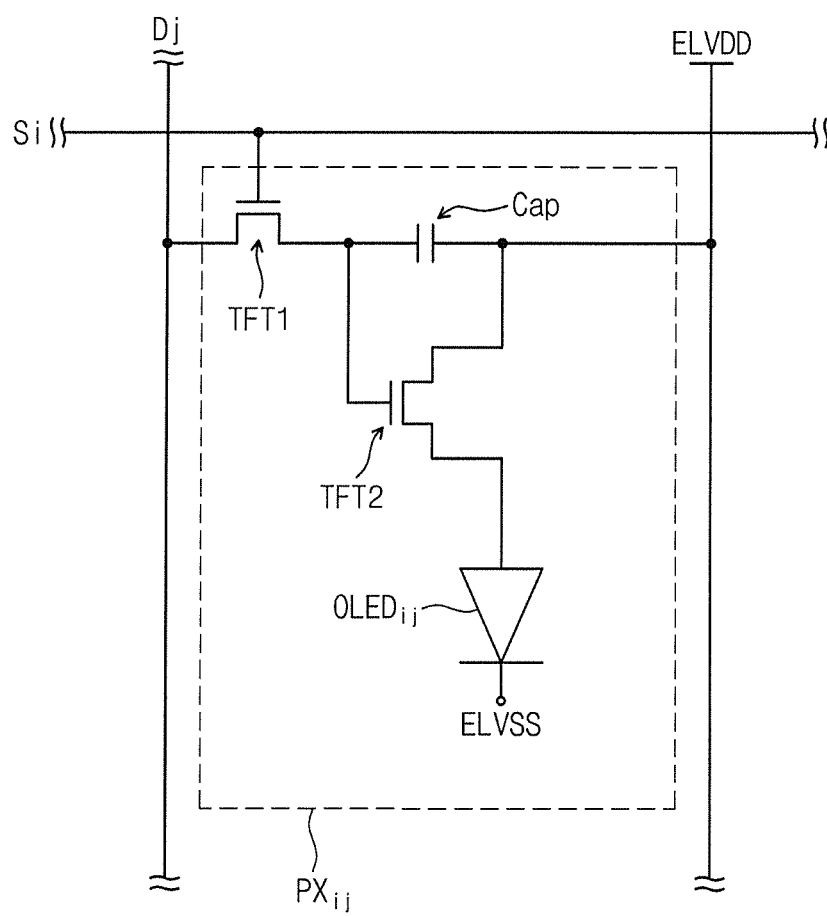


Fig. 3

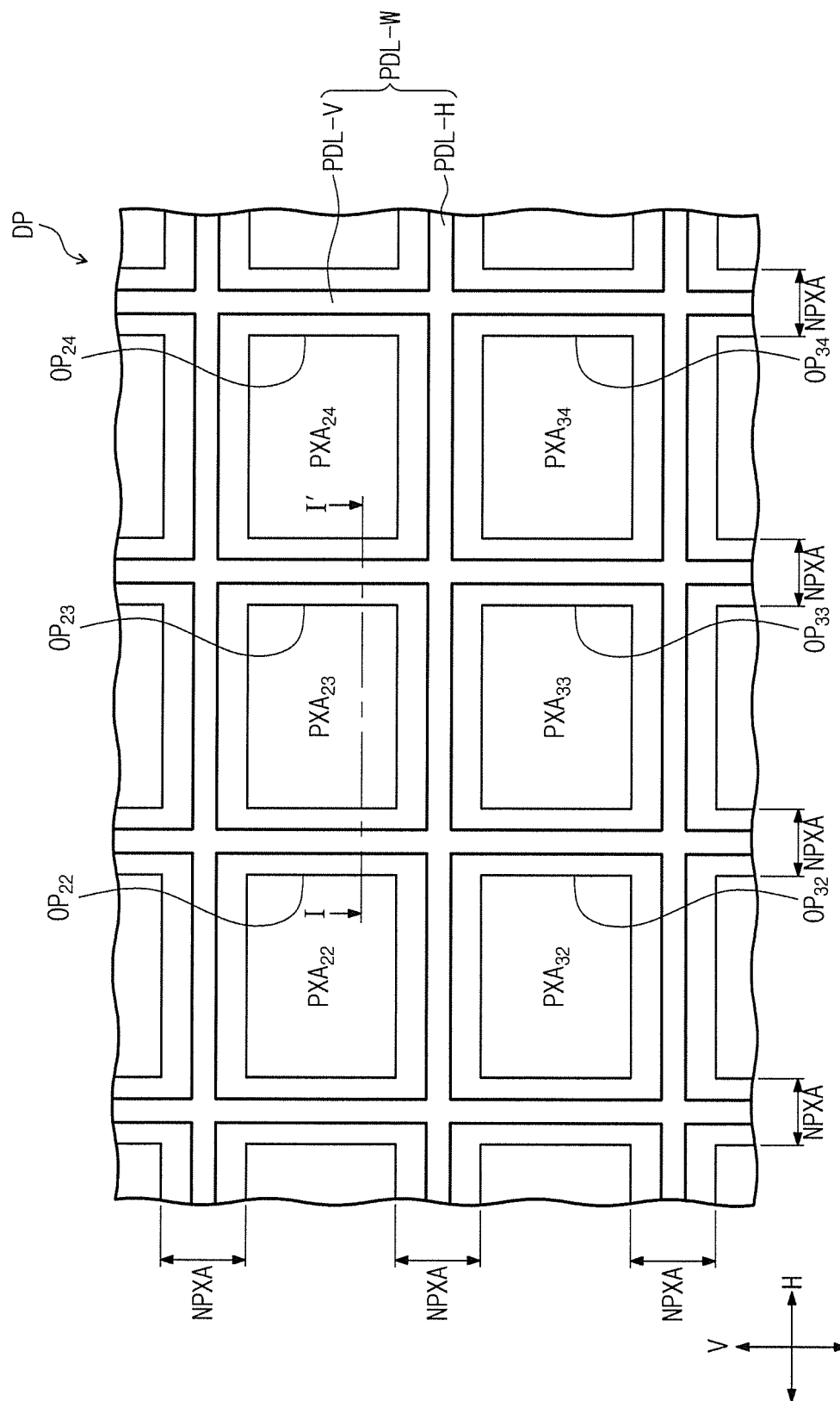


Fig. 4

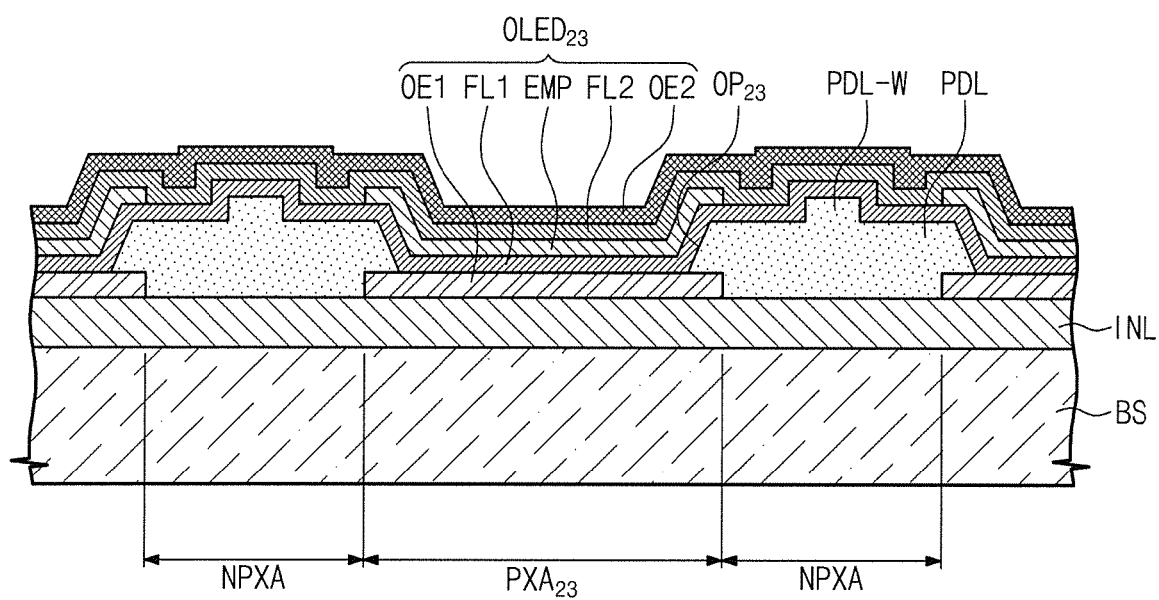


Fig. 5A

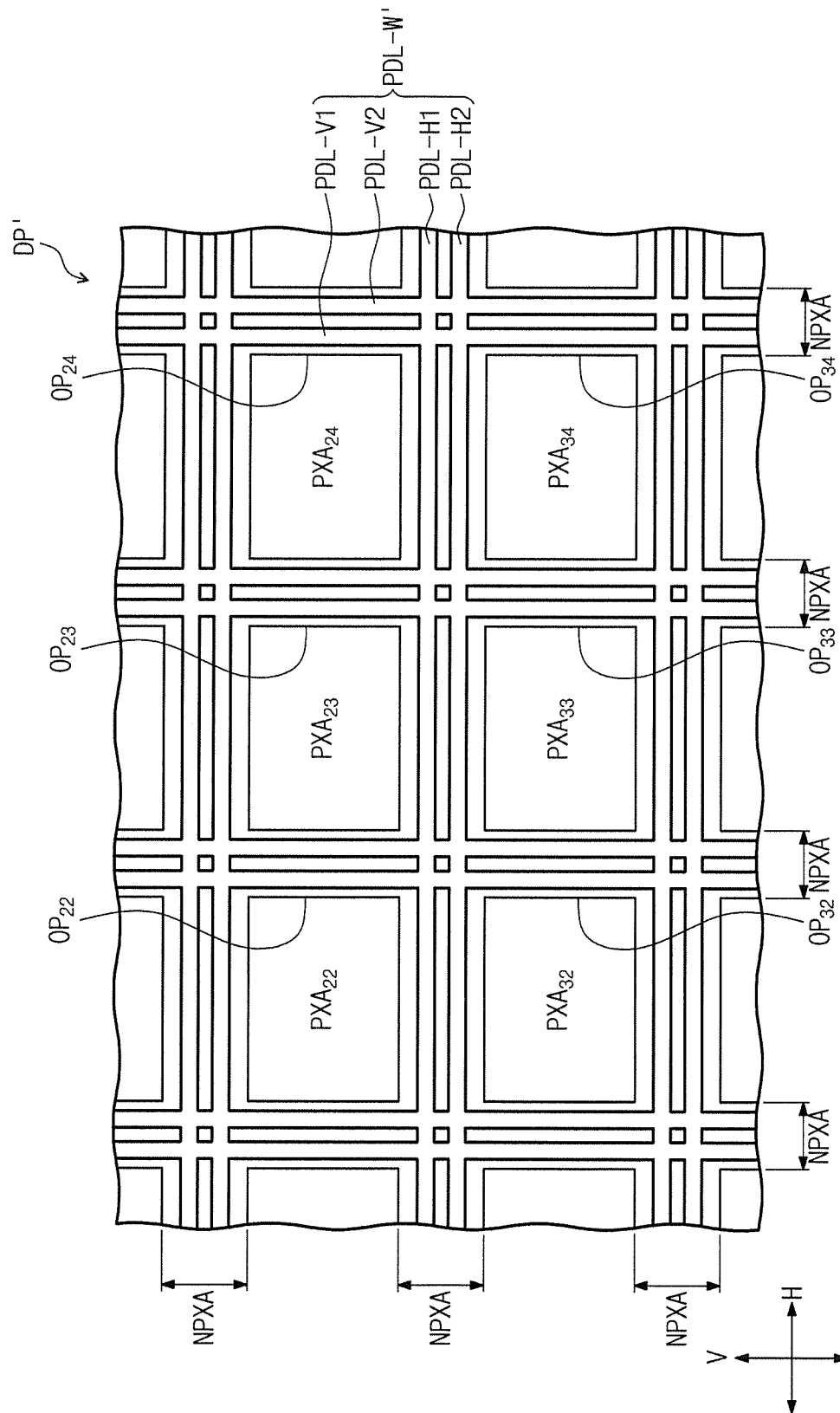


Fig. 5B

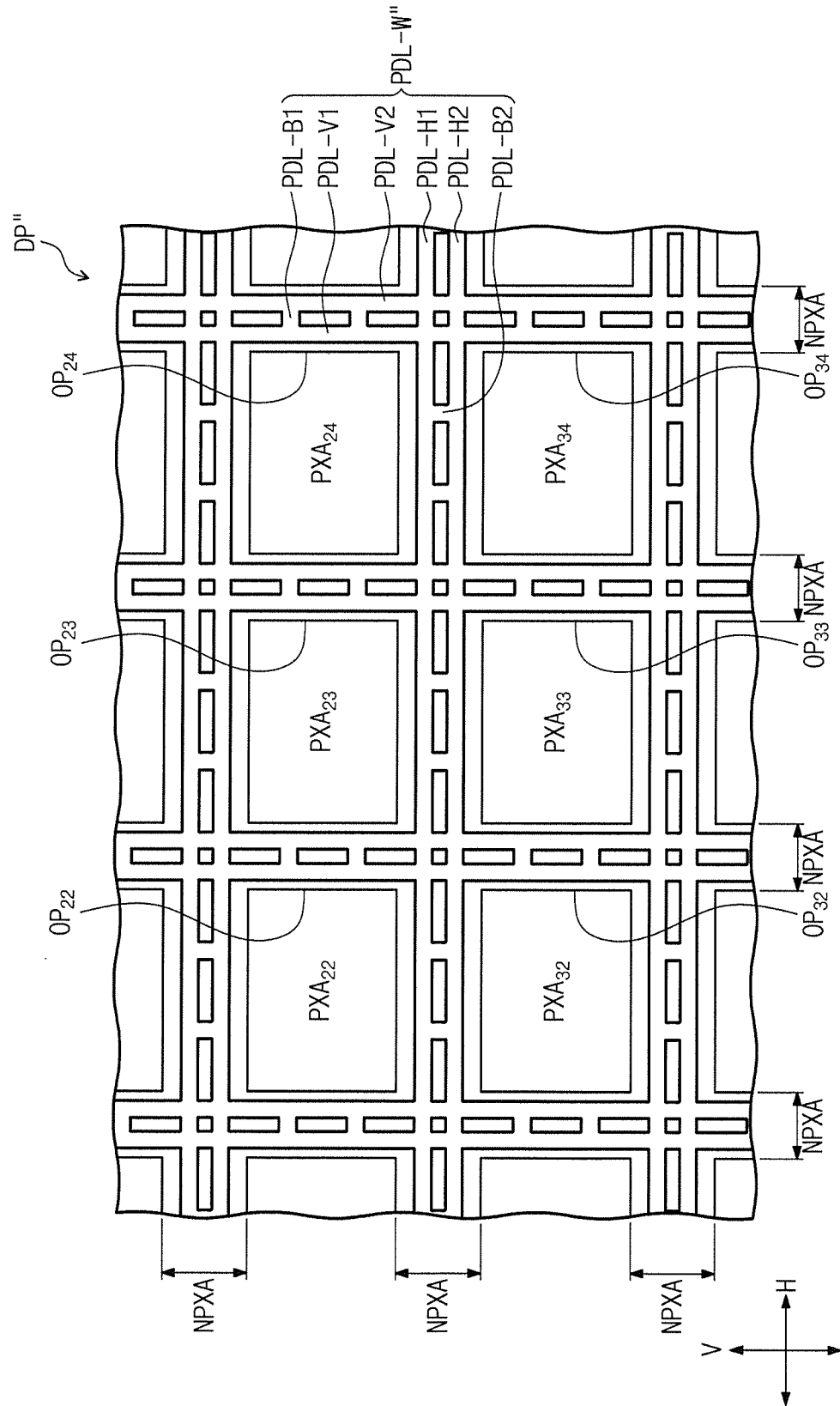




Fig. 5C

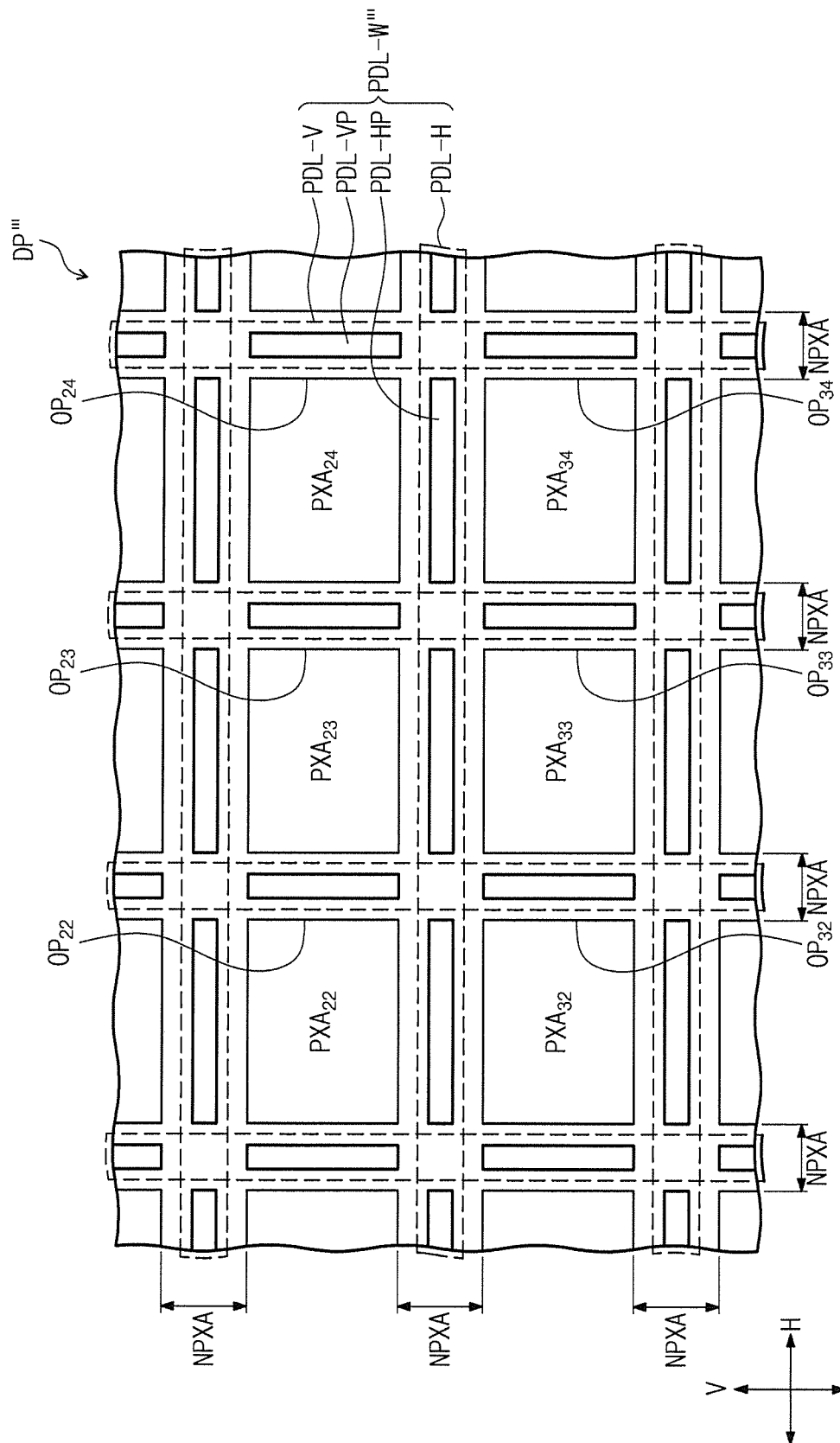


Fig. 6A

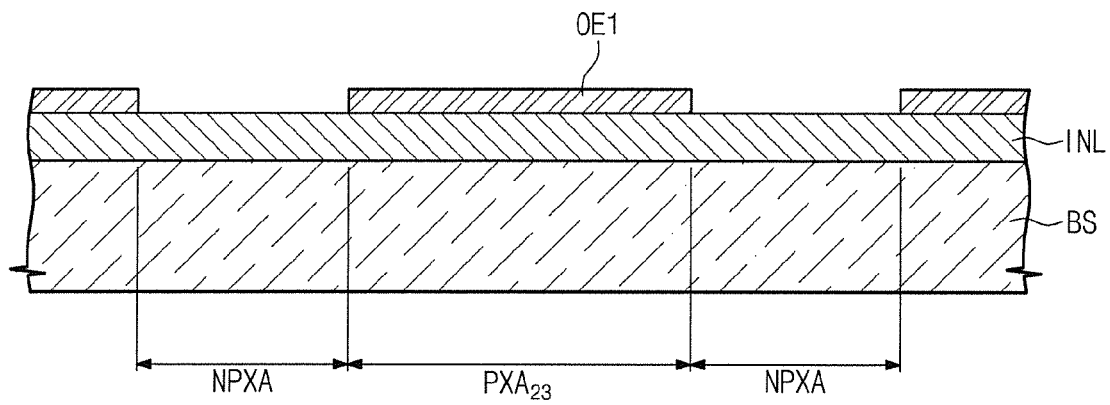


Fig. 6B

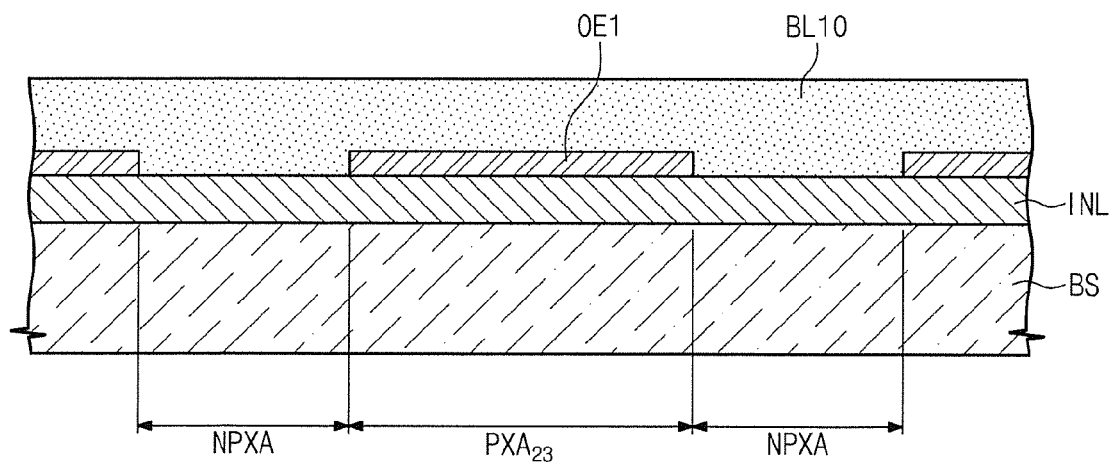


Fig. 6C

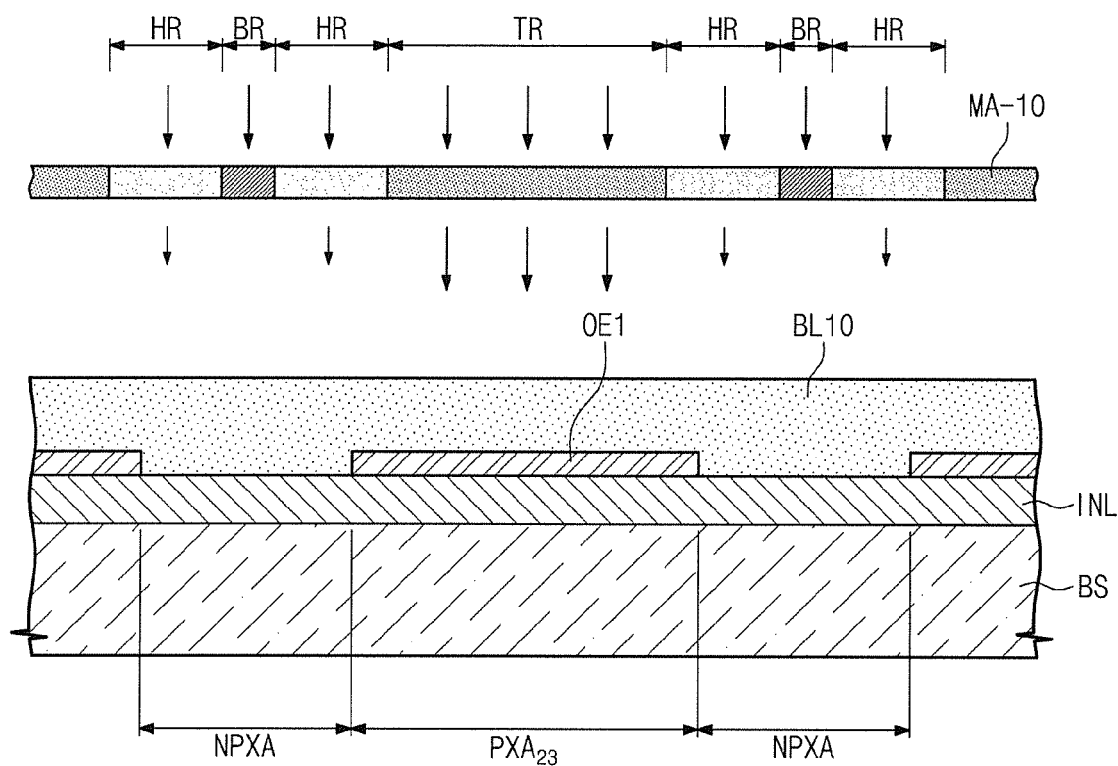
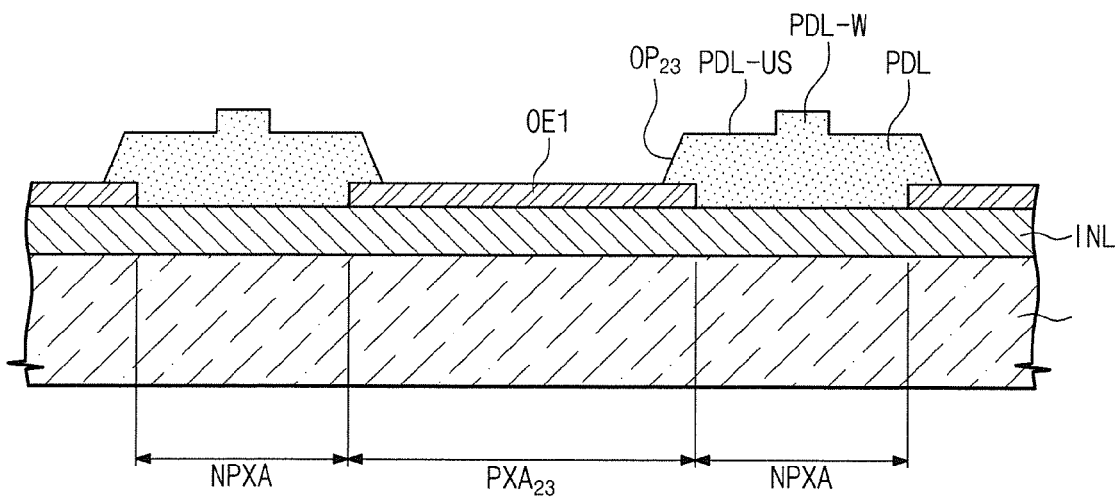


Fig. 6D



A cross-sectional view of a waveguide device. The device consists of a substrate (BS) with a bottom layer (INL). A central waveguide region (PDL) is formed on top of the INL layer. This central region is flanked by two side regions (PDL-W). The top surface of the device is covered by a layer (EM). The central waveguide region (PDL) is defined by a central core (OE1) and a cladding (FL1). The side regions (PDL-W) are defined by a core (OE1) and a cladding (FL1). The device is divided into three sections: NPXA (Non-Polarized X-ray Absorption) on the left and right, and PXA<sub>23</sub> (Polarized X-ray Absorption) in the center. The central section (PXA<sub>23</sub>) is flanked by two side sections (NPXA). The central section (PXA<sub>23</sub>) is flanked by two side sections (NPXA).

Fig. 6G

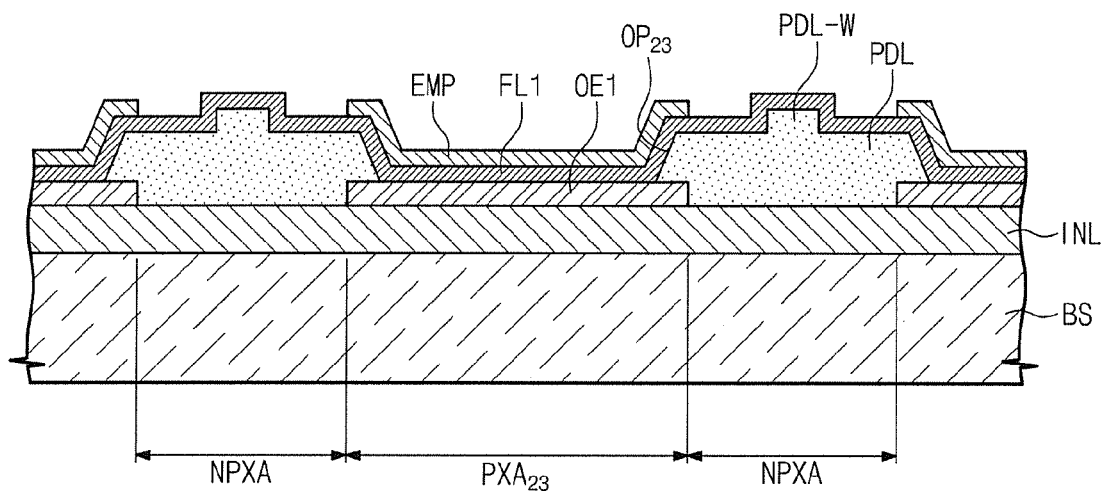


Fig. 6H

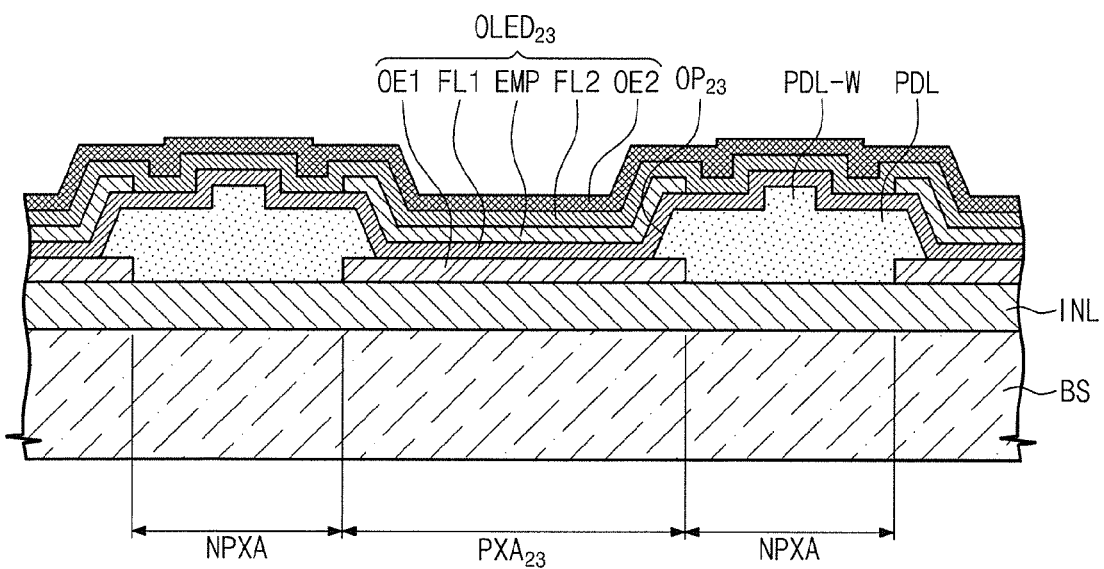




Fig. 8

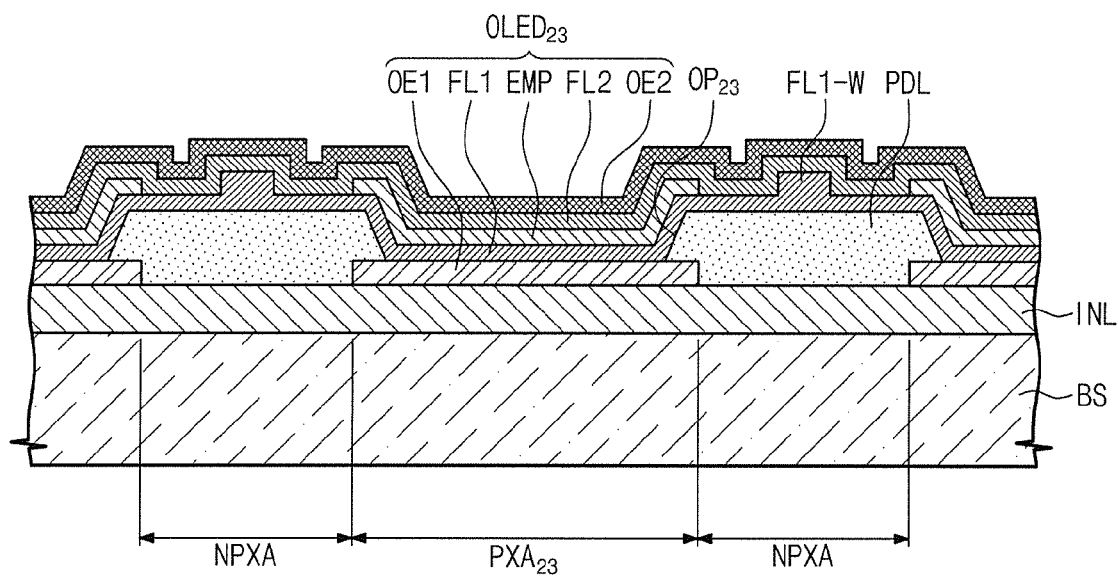


Fig. 9

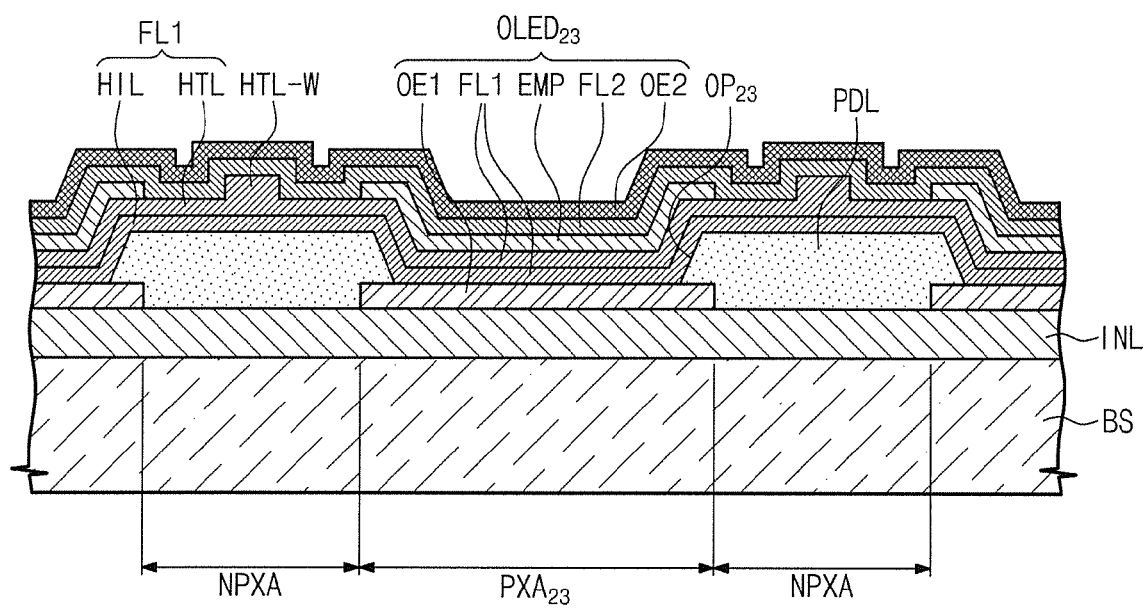




Fig. 10A

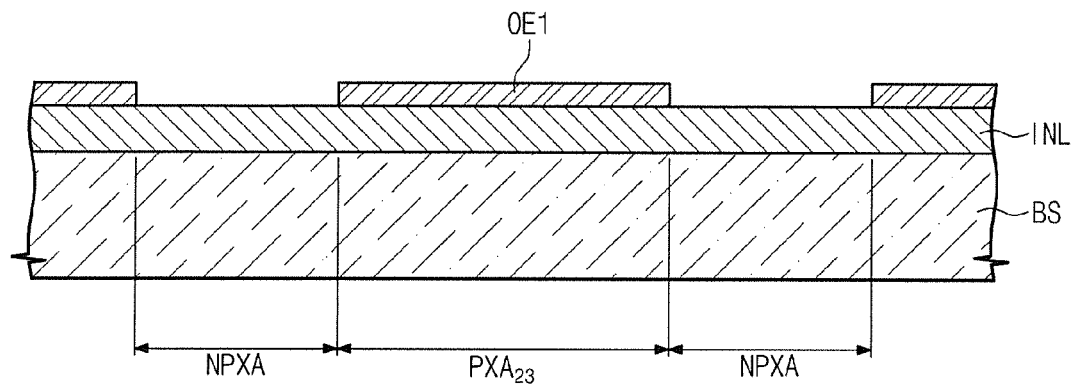


Fig. 10B

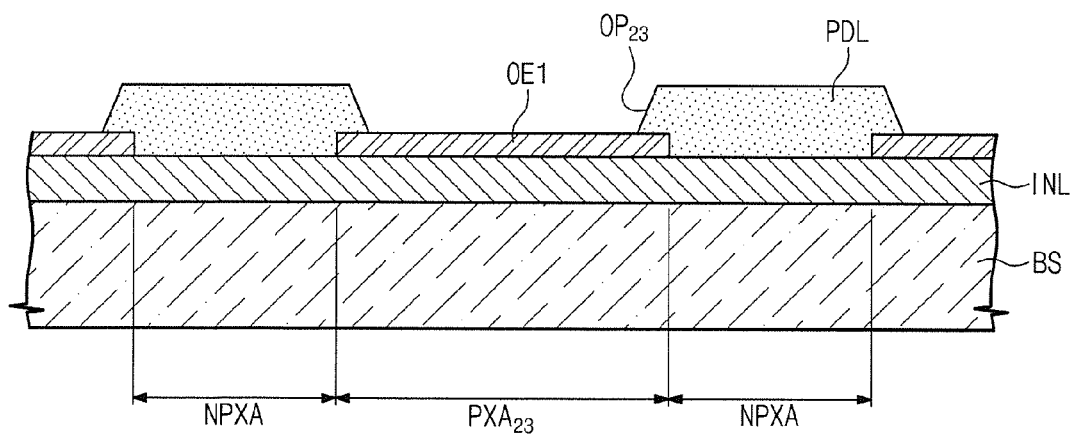


Fig. 10C

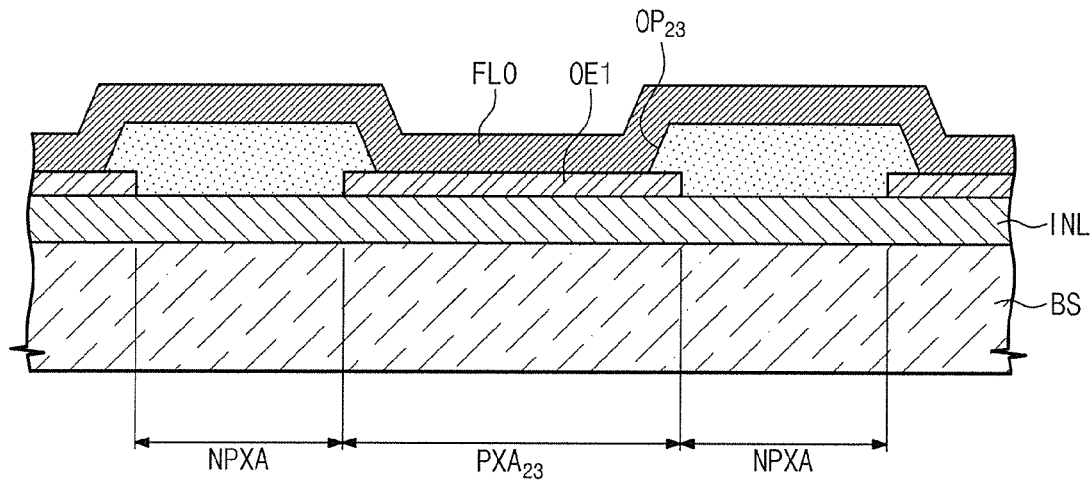


Fig. 10D

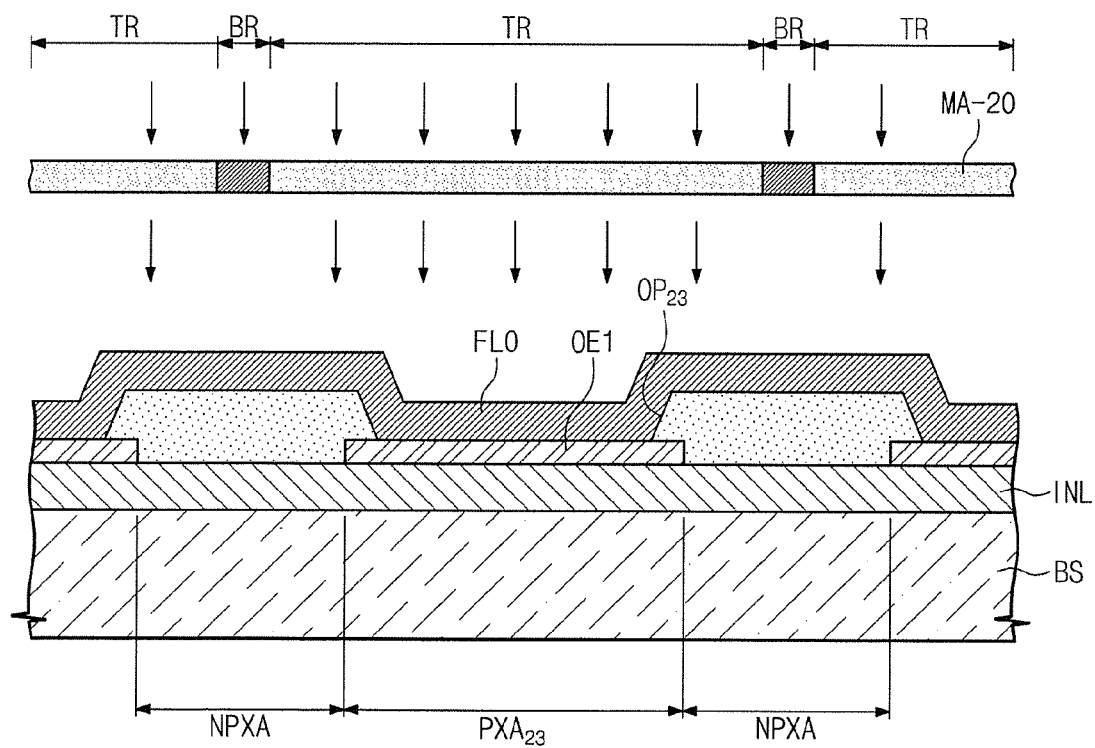


Fig. 10E

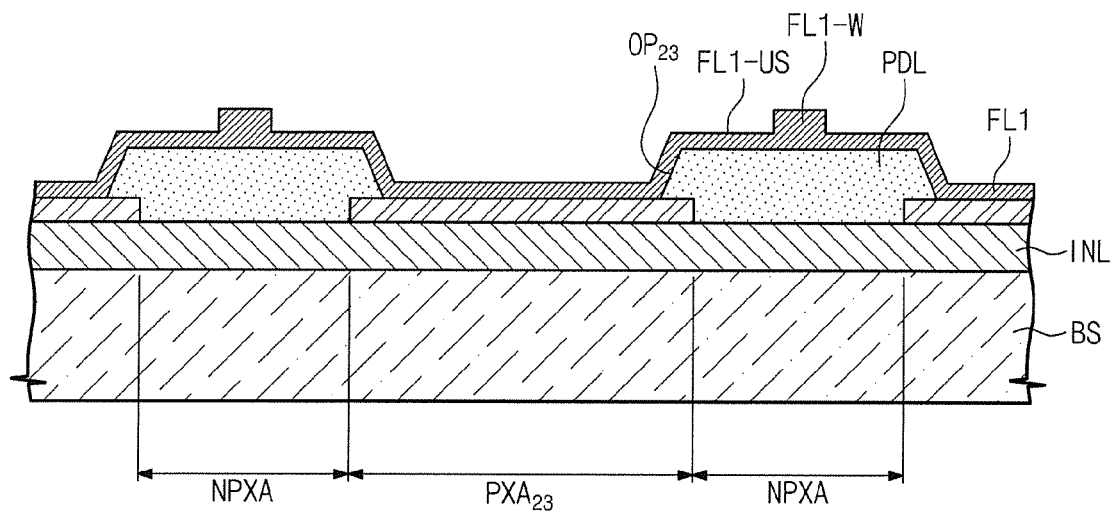


Fig. 10F

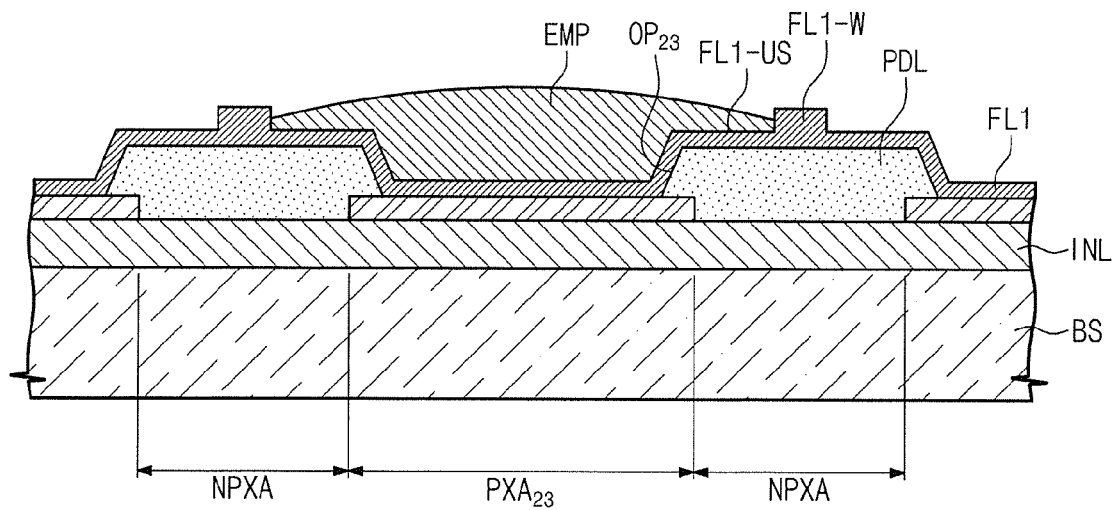


Fig. 10G

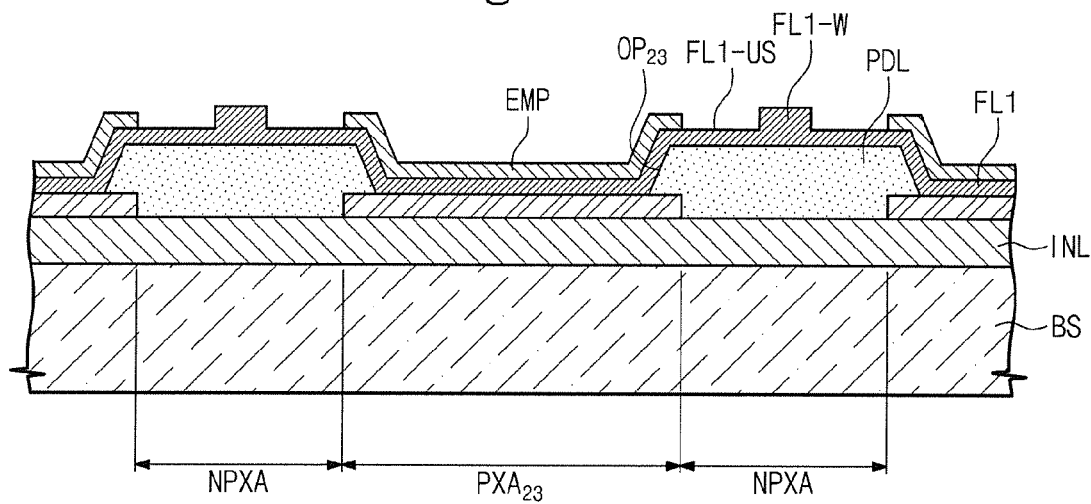
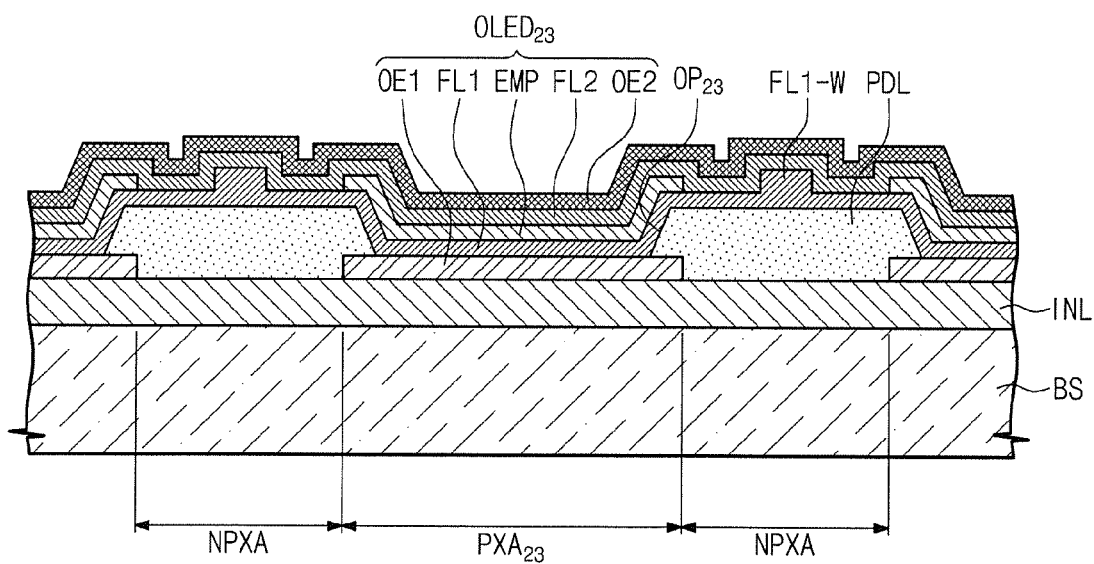


Fig. 10H



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# ORGANIC LIGHT EMITTING DISPLAY PANEL AND METHOD OF MANUFACTURING THE SAME

## CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to and the benefit of Korean Patent Application No. 10-2012-0105410, filed on Sep. 21, 2012, the entire contents of which are hereby incorporated by reference.

## BACKGROUND

### 1. Field

The present disclosure relates to an organic light emitting display panel and a method of manufacturing the same. More particularly, the present disclosure relates to an organic light emitting display panel including organic light emitting patterns formed of different materials and a method of manufacturing the organic light emitting display panel.

### 2. Description of the Related Art

An organic light emitting display includes an organic light emitting display panel and a driver that controls the organic light emitting display panel. The organic light emitting display panel includes a plurality of pixels each including an organic light emitting device. The organic light emitting device includes organic light emitting patterns and electrodes for applying driving voltages to the organic light emitting patterns. In addition, common electrodes are located between the organic light emitting patterns and the electrodes.

At least one portion of the pixels includes organic light emitting patterns formed of a material different from a material used to form organic light emitting patterns of another portion of the pixels. For example, one portion of the organic light emitting patterns may include a material to emit a red light, another portion of the organic light emitting patterns may include a material to emit a green light, still another portion of the organic light emitting patterns may include a material to emit a blue light, and yet another portion of the organic light emitting patterns may include a material to emit a white light.

## SUMMARY

Aspects of the present disclosure provide an organic light emitting display panel for reducing defects of a pixel, and a method of manufacturing the organic light emitting display panel.

One or more embodiments of the present invention provide an organic light emitting display panel that includes: a base substrate; a first electrode layer including a plurality of first electrodes on the base substrate; a pixel definition layer on the base substrate, having a plurality of openings to respectively expose the first electrodes, and including a partition wall protruding from a surface thereof; a first common layer covering the first electrodes and the pixel definition layer; an organic light emitting layer on the first common layer and including a plurality of organic light emitting patterns corresponding to the first electrodes, respectively; and a second electrode layer on the organic light emitting layer.

The first common layer may include at least one of a hole injection layer or a hole transfer layer.

The organic light emitting display panel may further include a second common layer between the organic light emitting layer and the second electrode layer.

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The second common layer may include at least one of an electron injection layer or an electron transfer layer.

The first electrodes may be in a matrix form with rows and columns, and the partition wall may include a first portion extending in a row direction and a second portion extending in a column direction. The first portion may be integrally formed with the second portion.

The first portion may be one of a plurality of first portions, each first portion may be between two first electrodes adjacent to each other in the column direction, and the second portion may be one of a plurality of second portions, each second portion may be between two first electrodes adjacent to each other in the row direction.

Additionally, one or more embodiments of the present invention may provide for a method of manufacturing an organic light emitting display panel that includes: forming a first electrode layer including a plurality of first electrodes on a base substrate; forming a pixel definition layer having a plurality of openings to respectively expose the first electrodes and including a partition wall protruding from a surface thereof; forming a first common layer covering the first electrodes and the pixel definition layer; providing an organic light emitting material in a liquid state to areas corresponding to the openings to form an organic light emitting layer including a plurality of organic light emitting patterns; and forming a second electrode layer on the organic light emitting layer.

The method may further include forming a second common layer between the organic light emitting layer and the second electrode layer to cover the organic light emitting layer.

The forming of the pixel definition layer may include: forming a base layer on the base substrate to cover the first electrodes; and patterning the base layer using a mask including a transmission area corresponding to the openings, a block area corresponding to the partition wall, and a semi-transmission area adjacent to the transmission area and the block area.

The organic light emitting material in the liquid state provided to portions of the areas corresponding to the openings may be different from an organic light emitting material in the liquid state provided to other portions of the areas corresponding to the openings.

Additionally, an organic light emitting display panel according to another embodiment of the present invention may include: a base substrate; a first electrode layer having a plurality of first electrodes on the base substrate; a pixel definition layer having a plurality of openings to respectively expose the first electrodes; a first common layer including a partition wall protruding from a surface thereof, the first common layer covering the first electrodes and the pixel definition layer, and the partition wall being overlapped with the pixel definition layer; an organic light emitting layer on the first common layer and including a plurality of organic light emitting patterns corresponding to the first electrodes, respectively; and a second electrode layer on the organic light emitting layer.

The first common layer may include at least one of a hole injection layer or a hole transfer layer.

The first common layer may include the hole injection layer and the hole transfer layer on the hole injection layer, and the partition wall protrudes from the hole injection layer.

The organic light emitting display panel may further include a second common layer between the organic light emitting layer and the second electrode layer.

The second common layer may include at least one of an electron injection layer or an electron transfer layer.

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The first electrodes may be in a matrix form with rows and columns, and the partition wall may include a first portion extending in a row direction and a second portion extending in a column direction.

The first portion of the partition may be integrally formed with the second portion of the partition wall.

The first portion may be one of a plurality of first portions, each first portion may be between two first electrodes adjacent to each other in the column direction, and the second portion may be one of a plurality of second portions, each second portion may be between two first electrodes adjacent to each other in the row direction.

Further, a method of manufacturing an organic light emitting display panel according to another embodiment includes: forming a first electrode layer including a plurality of first electrodes on a base substrate; forming a pixel definition layer having a plurality of openings to respectively expose the first electrodes; forming a first common layer including a partition wall protruding from a surface of an area of the first common layer overlapped with the pixel definition layer, the first common layer covering the first electrodes and the pixel definition layer; providing an organic light emitting material in a liquid state to areas corresponding to the openings to form an organic light emitting layer including a plurality of organic light emitting patterns; and forming a second electrode layer on the organic light emitting layer.

The method may further include forming a second common layer between the organic light emitting layer and the second electrode layer to cover the organic light emitting layer.

The forming of the first common layer may include: forming a base layer on the base substrate to cover the first electrodes; and patterning the base layer using a mask including a block area corresponding to the partition wall and a transmission area adjacent to the block area.

The base layer may include a first layer formed from a hole injection material and a second layer on the first layer and formed from a hole transfer material, and the partition wall may be formed by removing portions of the second layer in a thickness direction of the second layer.

The organic light emitting material in the liquid state provided to portions of the areas corresponding to the openings may be different from the organic light emitting material in the liquid state provided to other portions of the areas corresponding to the openings.

According to the above, one or more embodiments of the organic light emitting display panel includes the partition wall to prevent (or inhibit) different organic light emitting materials from being mixed with each other between adjacent light emitting areas. Thus, desired light colors may be generated by organic light emitting patterns respectively disposed in the light emitting areas.

According to one or more embodiments of the method of manufacturing the organic light emitting display panel, the organic light emitting material in the liquid state is provided to the areas respectively corresponding to the openings. The partition wall prevents (or inhibits) the organic light emitting material provided to one opening from being mixed with the organic light emitting material provided to another opening adjacent to the one opening.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The above and other aspects of the present invention will become readily apparent by reference to the following detailed description when considered in conjunction with the accompanying drawings, wherein:

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FIG. 1 is a block diagram showing an organic light emitting display according to an exemplary embodiment of the present invention;

FIG. 2 is an equivalent circuit diagram illustrating a pixel of FIG. 1;

FIG. 3 is a schematic plan view illustrating a display panel according to an exemplary embodiment of the present invention;

FIG. 4 is a schematic cross-sectional view taken along the line I-I' of FIG. 3;

FIGS. 5A to 5C are schematic plan views illustrating display panels according to other exemplary embodiments of the present invention;

FIGS. 6A to 6H are schematic cross-sectional views illustrating a method of manufacturing a display panel according to an exemplary embodiment of the present invention;

FIG. 7 is a schematic plan view illustrating a display panel according to another exemplary embodiment of the present invention;

FIG. 8 is a schematic cross-sectional view taken along the line II-II' of FIG. 7;

FIG. 9 is a schematic cross-sectional view illustrating a display panel according to another exemplary embodiment of the present invention; and

FIGS. 10A to 10H are schematic cross-sectional views illustrating a method of manufacturing a display panel according to another exemplary embodiment of the present invention.

#### DETAILED DESCRIPTION

When an element or layer is referred to as being “on”, “connected to” or “coupled to” another element or layer, it can be directly on, connected or coupled to the other element or layer, or one or more intervening elements or layers may be interposed therebetween. In contrast, when an element is referred to as being “directly on”, “directly connected to” or “directly coupled to” another element or layer, there are no intervening elements or layers present. Like numbers refer to like elements throughout. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

Although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

Spatially relative terms, such as “beneath”, “below”, “lower”, “above”, “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as “below” or “beneath” other elements or features would then be oriented “above” the other elements or features. Thus, the example term “below” may encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations), and the spatially relative descriptors used herein may be interpreted accordingly.

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The terminology used herein is for the purpose of describing particular embodiments only and should not limit the invention. As used herein, the singular forms, “a”, “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. The terms “includes” and/or “including”, when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. Further, terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

Hereinafter, the present invention will be explained in detail with reference to the accompanying drawings.

FIG. 1 is a block diagram illustrating an organic light emitting display according to an exemplary embodiment of the present invention, and FIG. 2 is an equivalent circuit diagram illustrating a pixel of FIG. 1.

Referring to FIG. 1, an organic light emitting display includes an organic light emitting display panel DP (hereinafter, referred to as display panel), a timing controller 100, a scan driver 200, and a data driver 300.

The display panel DP includes a base substrate BS (refer to FIG. 4), a plurality of scan lines S1 to Sn arranged on the base substrate BS, a plurality of data lines D1 to Dm arranged on the base substrate BS, and a plurality of pixels PX<sub>11</sub> to PX<sub>Nm</sub> each connected to a corresponding scan line of the scan lines S1 to Sn and to a corresponding data line of the data lines D1 to Dm.

The scan lines S1 to Sn may extend in a first direction H (e.g., a horizontal direction) on the base substrate BS, and may be spaced apart from each other in a second direction V (e.g., a vertical direction), which crosses (e.g., is perpendicular to) the first direction H. The data lines D1 to Dm are insulated from the scan lines S1 to Sn, and cross the scan lines S1 to Sn. The data lines D1 to Dm may extend in the second direction V, and may be spaced apart from each other in the first direction H.

The display panel DP may receive a first source voltage ELVDD and a second source voltage ELVSS from an external source (not shown). Each of the pixels PX<sub>11</sub> to PX<sub>Nm</sub> is turned on in response to a corresponding scan signal received from a corresponding scan line S1 to Sn. Each of the pixels PX<sub>11</sub> to PX<sub>Nm</sub> may receive the first source voltage ELVDD and the second source voltage ELVSS and generates a light in response to a corresponding data signal received from a corresponding data line D1 to Dm. The first source voltage ELVDD may have a voltage level higher than that of the second source voltage ELVSS.

Each of the pixels PX<sub>11</sub> to PX<sub>Nm</sub> includes at least one transistor, at least one capacitor, and an organic light emitting device. FIG. 2 shows the equivalent circuit diagram of a pixel PX<sub>ij</sub> connected to an i-th scan line Si of the scan lines S1 to Sn and a j-th data line Dj of the data lines D1 to Dm.

In FIG. 2, the pixel PX<sub>ij</sub> includes a first transistor TFT1, a second transistor TFT2, a capacitor Cap, and an organic light emitting device (e.g., an organic light emitting diode) OLED<sub>ij</sub>. The first transistor TFT1 includes a control electrode connected to the i-th scan line Si, an input electrode connected to the j-th data line Dj, and an output electrode. The

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first transistor TFT1 outputs a data signal applied through the j-th data line Dj in response to the scan signal applied to the i-th scan line Si.

The capacitor Cap includes a first electrode connected to the first transistor TFT1 and a second electrode applied with the first source voltage ELVDD. The capacitor Cap may be charged with the electric charge corresponding to a difference between a voltage corresponding to the data signal provided from the first transistor TFT1 and the first source voltage ELVDD.

The second transistor TFT2 includes a control electrode connected to the output electrode of the first transistor TFT1 and the first electrode of the capacitor Cap, an input electrode applied with the first source voltage ELVDD, and an output electrode. The output electrode of the second transistor TFT2 is connected to the organic light emitting device OLED<sub>ij</sub>.

The second transistor TFT2 controls a driving current flowing through the organic light emitting device OLED<sub>ij</sub> in accordance with the electric charge amount charged in the capacitor Cap. A turn-on time of the second transistor TFT2 is determined by the electric charge amount charged in the capacitor Cap. The output electrode of the second transistor TFT2 applies a voltage having a level lower than that of the first source voltage ELVDD to the organic light emitting device OLED<sub>ij</sub>.

The organic light emitting device OLED<sub>ij</sub> includes a first electrode connected to the second transistor TFT2 and a second electrode connected to receive the second source voltage ELVSS. The organic light emitting device OLED<sub>ij</sub> may include a first common layer, an organic light emitting pattern, and a second common layer, which are all between the first and second electrodes. The organic light emitting device OLED<sub>ij</sub> may emit light during the turn-on time of the second transistor TFT2. The light generated by the organic light emitting device OLED<sub>ij</sub> has a color determined by a material used to form the organic light emitting pattern. For example, the light emitted from the organic light emitting device OLED<sub>ij</sub> may have one of red, green, blue, or white colors.

The timing controller 100 may receive image signals and may convert the image signals to image data I<sub>DATA</sub> appropriate to an operation mode of the display panel DP. The timing controller 100 may output the image data I<sub>DATA</sub> and various control signals SCS and DCS.

The scan driver 200 may receive a scan driving control signal SCS from the timing controller 100 and may generate a plurality of scan signals in response to the scan driving control signal SCS. The scan signals may be sequentially applied to the scan lines S1 to Sn.

The data driver 300 may receive a data driving control signal DCS and the image data I<sub>DATA</sub> from the timing controller 100. The data driver 300 may generate a plurality of data signals according to the data driving control signal DCS and the image data I<sub>DATA</sub>. The data signals are applied to the data lines D1 to Dm.

FIG. 3 is a schematic plan view illustrating a display panel according to an exemplary embodiment of the present invention, and FIG. 4 is a schematic cross-sectional view taken along a line I-I' of FIG. 3. In particular, FIG. 3 illustrates six light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> respectively corresponding to six openings OP<sub>22</sub> to OP<sub>34</sub>, and FIG. 4 illustrates a schematic cross section of one of the six light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub>.

Referring to FIG. 3, the display panel DP includes light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> and a non-light emitting area NPXA adjacent to the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub>. The light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> may be surrounded (e.g., the perimeter may be surrounded) by the non-light

emitting area NPXA. The first electrodes of the organic light emitting device OLED<sub>11</sub> to OLED<sub>nm</sub> of the pixels PX<sub>11</sub> to PX<sub>nm</sub> are disposed in the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub>, respectively.

Referring to FIG. 4, an insulating layer INL is disposed on the surface of the base substrate BS. Although not shown in detail, the insulating layer INL may include a plurality of thin layers. The thin layers may include an inorganic thin layer and/or an organic thin layer. Thin film transistors may be formed between the surface of the base substrate BS and the insulating layer INL. The thin film transistors may be the first and second transistors TFT1 and TFT2 (refer to FIG. 2).

In FIG. 4, a pixel definition layer PDL including the opening OP<sub>23</sub> formed therethrough is disposed on the insulating layer INL. The opening OP<sub>23</sub> corresponds to the light emitting area PXA<sub>23</sub>. The organic light emitting device OLED<sub>23</sub> may be disposed on the insulating layer INL. The organic light emitting device OLED<sub>23</sub> may include a first electrode OE1, a first common layer FL1, an organic light emitting pattern EMP, a second common layer FL2, and a second electrode OE2. In the present exemplary embodiment, the first electrode OE1 and the second electrode OE2 may be referred to as a positive electrode and a negative electrode, respectively.

The first electrode OE1 is arranged corresponding to the light emitting area PXA<sub>23</sub>. The first electrode OE1 may receive the first source voltage ELVDD. The opening OP<sub>23</sub> may expose at least a portion of the first electrode OE1. Although not shown in the figures, the first electrodes OE1 respectively disposed in the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> may form a first electrode layer in the display panel.

According to one or more embodiments of the present invention, the pixel definition layer PDL includes a partition wall PDL-W protruding from a surface thereof. The partition wall PDL-W may be formed of the same material as the pixel definition layer PDL. The partition wall PDL-W may overlap with the pixel definition layer PDL, and may be disposed in the non-light emitting area NPXA.

Referring to back FIG. 3, the partition wall PDL-W includes a first portion PDL-H extended in a row direction (or first direction) H and a second portion PDL-V extended in a column direction (or second direction) V. Each of the first and second portions PDL-H and PDL-V may be provided in a plural number. The first portions PDL-H may be integrally formed with the second portions PDL-V. In this case, each of the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> is surrounded (e.g., the perimeter is surrounded) by the partition wall PDL-W when viewed in a plan view.

As shown in FIG. 4, the first common layer FL1 is located on the first electrode OE1 and the pixel definition layer PDL. Although not shown in the figures, the first common layer FL1, which may be integrally formed as a single unitary and individual unit, may be in the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> and the non-light emitting area NPXA.

The first common layer FL1, at least a part of which is on the partition wall PDL-W, may have a step difference shape in the non-light emitting area NPXA. The first common layer FL1 may include a hole injection layer. The hole injection layer may contact the first electrode OE1. In addition, the first common layer FL1 may further include a hole transfer layer on the hole injection layer.

The organic light emitting pattern EMP may be on the first common layer FL1, and corresponds to the light emitting area PXA<sub>23</sub>. Although not shown in the figures, the organic light emitting patterns EMP are respectively disposed in the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> to form an organic light emitting layer in the display panel DP.

The second common layer FL2 may be on the organic light emitting pattern EMP and the first common layer FL1. Although not shown in the figures, the second common layer FL2 integrally formed as a single unitary and individual unit may be in the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> and the non-light emitting area NPXA. The second common layer FL2 may include an electron injection layer. In addition, the second common layer FL2 may further include an electron transfer layer disposed between the organic light emitting pattern EMP and the electron injection layer. However, according to another exemplary embodiment, the second common layer FL2 may be omitted.

In FIG. 4, the second electrode OE2 is on the second common layer FL2, and corresponds to the light emitting area PXA<sub>23</sub>. Although not shown in the figures, the second electrodes OE2 respectively disposed in the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> may form a second electrode layer in the display panel DP. The second electrode OE2 may receive the second source voltage ELVSS.

In addition, a protective layer and/or a color filter layer may be disposed on the second electrode OE2. Another base substrate may be disposed on the second electrode OE2 to face the base substrate BS. The other base substrate may be a sealing substrate to protect the pixels PX<sub>11</sub> to PX<sub>nm</sub>.

FIGS. 5A to 5C are schematic plan views illustrating display panels according to other exemplary embodiments of the present invention.

Referring to FIG. 5A, a display panel DP' includes a partition wall PDL-W', which includes a plurality of first portions PDL-H1 and PDL-H2 and a plurality of second portions PDL-V1 and PDL-V2.

When viewed in a plan view, the first portions PDL-H1 and PDL-H2 are arranged between two light emitting areas adjacent to each other in the column direction V among the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub>. In addition, the second portions PDL-V1 and PDL-V2 are arranged between two light emitting areas adjacent to each other in the row direction H among the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> when viewed in a plan view. The first portions PDL-H1 and PDL-H2 may be integrally formed with the second portions PDL-V1 and PDL-V2.

Referring to FIG. 5B, a display panel DP'' includes a partition wall PDL-W'', which includes the first portions PDL-H1 and PDL-H2 and the second portions PDL-V1 and PDL-V2. The partition wall PDL-W'' further includes a first bridge portion PDL-B1 to connect the first portions PDL-H1 and PDL-H2 to each other. In addition, the partition wall PDL-W'' further includes a second bridge portion PDL-B2 to connect the second portions PDL-V1 and PDL-V2 to each other.

Referring to FIG. 5C, a display panel DP''' includes a first portion PDL-H, which may include a plurality of first patterns PDL-HP spaced apart from each other, and includes the second portion PDL-V, which may include a plurality of second patterns PDL-VP spaced apart from each other. When viewed in a plan view, each of the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> is surrounded by a portion of the first patterns PDL-HP and a portion of the second patterns PDL-VP.

FIGS. 6A to 6H are schematic cross-sectional views illustrating a method of manufacturing a display panel according to an exemplary embodiment of the present invention. FIGS. 6A to 6H show schematic cross sections corresponding to the light emitting area PXA<sub>23</sub> shown in FIG. 4.

Referring to FIG. 6A, the first electrode OE1 is formed on the base substrate BS. An area of the base substrate BS, in which the first electrode OE1 is formed, is referred to as the light emitting area PXA<sub>23</sub>, and the area adjacent to the light emitting area PXA<sub>23</sub> is referred to as the non-light emitting



area NPXA. The first electrode OE1 is disposed on the insulating layer INL, which is disposed on the base substrate BS.

The insulating layer INL may include the thin layers sequentially stacked one on another. In addition, a thin film transistor may be formed on the base substrate BS before the first electrode OE1 is formed. The thin film transistor may be formed by deposition, exposure, and development processes. Any one of the thin layers included in the insulating layer INL may serve as a portion of the thin film transistor.

Referring to FIG. 6B, a base layer BL10 is formed on the insulating layer INL to cover the first electrode OE1. The base layer BL10 is patterned to define the pixel definition layer including the opening and the partition wall.

Referring to FIG. 6C, the base layer BL10 is patterned through an exposure and development process using a mask MA-10. The mask MA-10 may be a slit mask or a diffraction mask, and may include a transmission area TR, a block area BR, and a semi-transmission area HR adjacent to the transmission area TR and the block area BR. The transmission area TR transmits incident light to the base layer BL10, the block area BR blocks the incident light to the base layer BL10, and the semi-transmission area HR transmits a portion of the incident light to the base layer BL10. The arrow shown in FIG. 6C indicates the incident light.

The mask MA-10 may be disposed to allow the transmission area TR to correspond to the area in which the opening is formed, the block area BR to correspond to the area in which the partition wall is formed, and the semi-transmission area HR to correspond to an other area. The area in which the opening is formed corresponds to the light emitting area PXA<sub>23</sub>, and the area in which the partition wall is formed and the other area correspond to the non-light emitting area NPXA.

FIG. 6D shows the base layer BL10 after the exposure process is performed. Here, the pixel definition layer PDL including the opening OP<sub>23</sub> and the partition wall PDL-W is formed from the base layer BL10. The base layer BL10 has different thicknesses in different areas thereof. The opening OP<sub>23</sub> may be formed by completely removing the base layer BL10 in a thickness direction, the partition wall PDL-W may be formed by not removing the base layer BL10, and portions that form a surface PDL-US of the pixel definition layer PDL may be formed by partially removing the base layer BL10.

Referring to FIG. 6E, the first common layer FL1 is formed on the pixel definition layer PDL. The first common layer FL1 may include the hole injection layer. In addition, the first common layer FL1 may further include the hole transfer layer disposed on the hole injection layer.

Referring to FIG. 6F, an organic light emitting material EM in a liquid state is disposed on the first common layer FL1. The organic light emitting material EM in the liquid state is disposed to correspond to the opening OP<sub>23</sub> of the pixel definition layer PDL. The organic light emitting material EM in the liquid state may be provided by, for example, an inkjet printing method or a nozzle printing method.

The partition wall PDL-W prevents (or inhibits) the organic light emitting material EM from flowing into adjacent light emitting areas PXA<sub>22</sub> and PXA<sub>24</sub> (refer to FIG. 3) from the light emitting area PXA<sub>23</sub> even if an amount of the organic light emitting material EM provided to the light emitting area PXA<sub>23</sub> is more (e.g., much more) than a reference amount. The reference amount is determined according to the area of the opening OP<sub>23</sub> and the area of the organic light emitting pattern EMP. The partition walls PDL-W shown in FIG. 5A to 5C have a similar function as the above-mentioned partition wall PDL-W. The adjacent light emitting areas PXA<sub>22</sub> and PXA<sub>24</sub> may be provided with organic light emitting materials

that are different materials from the organic light emitting material provided to the light emitting area PXA<sub>23</sub>. Accordingly, by preventing the organic light emitting material from flowing into adjacent light emitting areas, the different organic light emitting materials are prevented from mixing.

FIG. 6G shows the organic light emitting material EM after a solvent has been evaporated. The light emitting material EM (from which the solvent is evaporated) forms the organic light emitting pattern EMP.

Then, the second common layer FL2 is formed on the first common layer FL1 to cover the organic light emitting pattern EMP, and the second electrode OE2 is formed on the second common layer FL2. When the processes are completed, the organic light emitting display panel is manufactured as shown in FIG. 6H. The second common layer FL2 may include at least one of the electron injection layer or the electron transfer layer. In addition, the second common layer FL2 may be omitted.

FIG. 7 is a schematic plan view illustrating a display panel according to another exemplary embodiment of the present invention, and FIG. 8 is a schematic cross-sectional view taken along the line II-II' of FIG. 7. In FIGS. 7 and 8, the same (or similar) reference numerals denote the same elements in FIGS. 1 to 5C, and thus, detailed descriptions of the same elements will be given by way of reference to the above-descriptions.

Referring to FIG. 7, a display panel DP10 is divided into a plurality of light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> and a non-light emitting area NPXA adjacent to the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub>. The light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> are surrounded by the non-light emitting area NPXA.

Referring to FIG. 8, an insulating layer INL is disposed on a surface of the base substrate BS. Although not shown in detail, the insulating layer INL may include a plurality of thin layers.

A pixel definition layer PDL including an opening OP<sub>23</sub> is disposed on the insulating layer INL. The opening OP<sub>23</sub> corresponds to the opening OP<sub>23</sub>. The organic light emitting device OLED<sub>23</sub> may be disposed on the insulating layer INL.

The first electrode OE1 is disposed corresponding to the light emitting area PXA<sub>23</sub>. The first electrode OE1 may receive the first source voltage ELVDD (refer to FIG. 1). The opening OP<sub>23</sub> may expose at least a portion of the first electrode OE1.

The first common layer FL1 may be disposed on the first electrode OE1 and the pixel definition layer PDL. The first common layer FL1 may include a hole injection layer. The first common layer FL1, which may be integrally formed as a single unitary and individual unit, may be disposed in the light emitting areas PXA<sub>22</sub> to PXA<sub>34</sub> and the non-light emitting area NPXA.

The first common layer FL1 may include a partition wall FL1-W protruding from a surface thereof. The partition wall FL1-W may be formed of the same material as the first common layer FL1. The partition wall FL1-W may overlap with the pixel definition layer PDL. That is, the partition wall FL1-W may be disposed in the non-light emitting area NPXA.

Referring to back FIG. 7, the partition wall FL1-W may include a first portion FL1-H extending in the row direction H, and a second portion FL1-V extending in the column direction V. According to other embodiments of the present invention, the partition wall FL1-W may have similar shapes to the pixel defining layer walls PDL-W shown in FIGS. 5A to 5C.

As shown in FIG. 8, the organic light emitting pattern EMP may be disposed on the first common layer FL1, and may

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correspond to the light emitting area  $PXA_{23}$ . The second common layer FL2 may be disposed on the organic light emitting pattern EMP and the first common layer FL1. However, according to another exemplary embodiment, the second common layer FL2 may be omitted.

The second electrode OE2 may be disposed on the second common layer FL2. The second electrode OE2 may receive the second source voltage ELVSS (refer to FIG. 1).

FIG. 9 is a schematic cross-sectional view illustrating a display panel according to another exemplary embodiment of the present invention. In FIG. 9, the same (or similar) reference numerals denote the same elements in FIGS. 7 and 8, and thus detailed descriptions of the same elements will be given by way of reference to the above descriptions.

Referring to FIG. 9, the first common layer FL1 includes a hole injection layer HIL disposed on the first electrode OE1 and the pixel definition layer PDL, and a hole transfer layer HTL disposed on the hole injection layer HIL. The hole transfer layer HTL may include a partition wall HTL-W protruding from a surface thereof. The partition wall HTL-W may be formed of the same material as the hole transfer layer HTL. The second common layer FL2, which may be on the partition wall HTL-W, may have a step difference shape in the non-light emitting area NPXA.

FIGS. 10A to 10H are schematic cross-sectional views illustrating a method of manufacturing a display panel according to another exemplary embodiment of the present invention. In FIGS. 10A to 10H, the same (or similar) reference numerals denote the same elements in FIGS. 6A to 6H, and thus, detailed descriptions of the same elements will be given by way of reference to the above descriptions.

Referring to FIG. 10A, a first electrode OE1 is formed on a base substrate BS. An area of the base substrate BS, in which the first electrode OE1 is formed, is referred to as the light emitting area  $PXA_{23}$ , and the area adjacent to the light emitting area  $PXA_{23}$  is referred to as the non-light emitting area NPXA. The first electrode OE1 may be formed on the insulating layer INL disposed on the base substrate BS.

Referring to FIG. 10B, a pixel definition layer PDL including the opening  $OP_{23}$  formed therethrough is disposed on the insulating layer INL. The pixel definition layer PDL may be formed from a base layer through an exposure and development process using a mask (not shown). The mask may be a slit mask or a diffraction mask, and may include a transmission area and a blocking area. The opening  $OP_{23}$  may be formed in an area corresponding to the transmission area of the mask, and area other than the area for the opening  $OP_{23}$  may be formed in an area corresponding to the block area of the mask.

Referring to FIG. 10C, the base layer FL0 is formed on the insulating layer INL to cover the pixel definition layer PDL and the first electrode OE1. The base layer FL0 may be formed from a hole injection material, and may have a first thickness. The base layer FL0 may include a first layer formed from a hole injection material, and may include a second layer disposed on the first layer and formed from a hole transfer material.

The base layer FL0 may be patterned through an exposure and development processes. As shown in FIG. 10D, the base layer FL0 is exposed to the light using a mask MA-20 including the transmission area TR and the block area BR. The block area BR may be located at a position corresponding to an area in which the partition wall is formed, and the transmission area TR may be located at a position corresponding to the other areas.

FIG. 10E shows the base layer FL0 after the exposure process. According to an embodiment of the present inven-

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tion, the first common layer FL1 is formed from the base layer FL0 and has the partition wall FL1-W. Here, the base layer FL0 has a different thickness in areas corresponding to the partition wall FL1-W. That is, the partition wall FL1-W corresponds to an area from which the base layer FL0 is not removed and has the first thickness. Portions that form a surface FL1-US of the first common layer FL1, from which the base layer FL0 is partially removed, has a second thickness smaller than the first thickness.

As shown in FIG. 10F, an organic light emitting material EM in a liquid state may be disposed onto the first common layer FL1. The organic light emitting material EM in the liquid state may be disposed to correspond to the opening  $OP_{23}$  of the pixel definition layer PDL. The organic light emitting material EM in the liquid state may be provided by, for example, an inkjet printing method or a nozzle printing method.

The partition wall PDL-W prevents (or inhibits) the organic light emitting material EM from flowing into adjacent light emitting areas  $PXA_{22}$  and  $PXA_{24}$  (refer to FIG. 7) from the light emitting area  $PXA_{23}$ .

FIG. 10G shows the organic light emitting material EM from after a solvent has been evaporated. The light emitting material EM (from which the solvent is evaporated) forms the organic light emitting pattern EMP.

Then, the second common layer FL2 may be formed on the first common layer FL1 to cover the organic light emitting pattern EMP, and the second electrode OE2 may be formed on the second common layer FL2. When the above processes are completed, the organic light emitting display panel is manufactured as shown in FIG. 10H. The second common layer FL2 may include at least one of the electron injection layer or the electron transfer layer. In addition, the second common layer FL2 may be omitted.

Although various exemplary embodiments of the present invention have been described, it is understood that the present invention should not be limited to these exemplary embodiments but various changes and modifications can be made by one ordinary skilled in the art within the spirit and scope of the appended claims and their equivalents.

What is claimed is:

1. An organic light emitting display panel comprising:

- a base substrate;
- a first electrode layer having a plurality of first electrodes on the base substrate;
- a pixel definition layer having a plurality of openings to respectively expose the first electrodes;
- a first common layer comprising a partition wall protruding from and integrally formed with a surface thereof, the first common layer covering the first electrodes and the pixel definition layer, and the partition wall being overlapped with the pixel definition layer;
- an organic light emitting layer on the first common layer and comprising a plurality of organic light emitting patterns corresponding to the first electrodes, respectively; and
- a second electrode layer on the organic light emitting layer.

2. The organic light emitting display panel of claim 1, wherein the first common layer comprises at least one of a hole injection layer or a hole transfer layer.

3. The organic light emitting display panel of claim 2, wherein the first common layer comprises the hole injection layer and the hole transfer layer on the hole injection layer, and the partition wall protrudes from the hole injection layer.

4. The organic light emitting display panel of claim 2, further comprising a second common layer between the organic light emitting layer and the second electrode layer.

5. The organic light emitting display panel of claim 4, wherein the second common layer comprises at least one of an electron injection layer or an electron transfer layer.

6. The organic light emitting display panel of claim 1, wherein the first electrodes are in a matrix form with rows and columns, and the partition wall comprises a first portion extending in a row direction and a second portion extending in a column direction.

7. The organic light emitting display panel of claim 6, wherein the first portion of the partition is integrally formed with the second portion of the partition wall.

8. The organic light emitting display panel of claim 6, wherein the first portion is one of a plurality of first portions, each first portion being between two first electrodes adjacent to each other in the column direction, and

wherein the second portion is one of a plurality of second portions, each second portion being between two first electrodes adjacent to each other in the row direction.

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